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PATENT APPLICATION

ATTORNEY DOCKET NO. 200304264-1

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Thanh T. TRAN et al. **Confirmation No.:** 8851

Application No.: 09/191,629 **Examiner:** P. M. Natnael

Filing Date: 11/13/1998 **Group Art Unit:** 2614

Title: METHOD AND APPARATUS FOR TRANSMITTING DIGITAL TELEVISION DATA (AS AMENDED)

Mail Stop Appeal Brief-Patents
Commissioner For Patents
PO Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL OF APPEAL BRIEF

Sir:

Transmitted herewith is the Appeal Brief in this application with respect to the Notice of Appeal filed on **06/21/2005**.

The fee for filing this Appeal Brief is (37 CFR 1.17(c)) $500.00.

(complete (a) or (b) as applicable)

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136(a) apply.

( ) (a) Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)-(d) for the total number of months checked below:

( )	one month	$120.00
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( ) The extension fee has already been filled in this application.

(X) (b) Applicant believes that no extension of time is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

Please charge to Deposit Account **08-2025** the sum of **$500.00**. At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally please charge any fees to Deposit Account 08-2025 under 37 CFR 1.16 through 1.21 inclusive, and any other sections in Title 37 of the Code of Federal Regulations that may regulate fees. A duplicate copy of this sheet is enclosed.

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Number of pages: 32

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Respectfully submitted,

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appellants:	Thanh T. TRAN et al.	§	Confirmation No.:	8851
Serial No.:	09/191,629	§	Group Art Unit:	2614
Filed:	11/13/1998	§	Examiner:	P. M. Natnael
For:	Method And Apparatus For Transmitting Digital Television Data (As Amended)	§	Docket No.:	200304264-1

APPEAL BRIEF

Mail Stop Appeal Brief – Patents
Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Date: August 19, 2005

Sir:

Appellants hereby submit this Appeal Brief in connection with the above-identified application. A Notice of Appeal was filed via facsimile on June 21, 2005.

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I. REAL PARTY IN INTEREST

The real party in interest is the Hewlett-Packard Development Company (HPDC), a Texas Limited Partnership, having its principal place of business in Houston, Texas, through its merger with Compaq Computer Corporation (CCC) which owned Compaq Information Technologies Group, L.P. (CITG). The Assignment from the inventors to CCC was recorded on February 8, 1999, at Reel/Frame 9754/0459. The Assignment from CCC to CITG was recorded on January 8, 2002, at Reel/Frame 012458/0942. The Change of Name document was recorded on December 2, 2003, at Reel/Frame 014177/0428.

II. RELATED APPEALS AND INTERFERENCES

Appellants are unaware of any related appeals or interferences.

III. STATUS OF THE CLAIMS

Originally filed claims:	1-61.
Claim cancellations:	5, 7, 19, 25-33, 39, 47 and 53-61.
Added claims:	None.
Presently pending claims:	1-4, 6, 8-18, 20-24, 34-38, 40-46 and 48-52.
Presently appealed claims:	1-4, 6, 8-18, 20-24, 34-38 and 40-46.

IV. STATUS OF THE AMENDMENTS

No claims were amended after the Office action dated February 25, 2005.

V. SUMMARY OF THE CLAIMED SUBJECT MATTER

The various embodiments described in the specification are directed to a method and apparatus for transferring progressive scan digital television data on a peripheral component interconnect bus with non-tearing.[1] At least some of the illustrative embodiments are a method comprising storing incoming frames of digital television data in a first frame buffer of an interface logic,[2] reading outgoing frames of digital television data from a second frame buffer of the interface logic,[3] monitoring a feedback signal provided by a graphics controller coupled to the system (the monitoring by the interface logic and the feedback signal indicates whether a programmed position of a display device has been refreshed),[4] and transmitting the outgoing frames of digital television data in the second frame buffer to the graphics controller to be displayed on the display device when the programmed position of the display device is refreshed.[5]

Other illustrative embodiments are a system comprising a central processing unit (CPU),[6] a graphics controller coupled to the CPU,[7] a local bus coupled to the CPU and graphics controller,[8] and digital television/local bus interface logic coupled to the graphics controller by way of the local bus.[9] The digital television/local bus interface logic comprises a digital television interface that receives incoming digital television data,[10] a local bus interface that transmits

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[1] Specification original title. The title has been amended to read "method and apparatus for transmitting digital television data."

[2] Specification Page 7, lines 18-20; Figure 5. Hereinafter, cites to the specification take the form ([page]/[line numbers]). So, for example, this citation in the shorthand notation reads: (7/18-20).

[3] (7/ 26-29); Figure 6.

[4] (5/33-6/2); Figure 6.

[5] (7/33-8/2); Figure 6.

[6] (3/30); Figure 2.

[7] (5/21); Figure 2.

[8] (5/18); Figure 2.

[9] (5/13-14); Figure 2.

[10] (7/17); Figure 3.

outgoing digital television data to the graphics controller over the local bus,[11] a first frame buffer that stores the incoming digital television data and the outgoing digital television data in an alternating manner,[12] a second frame buffer that stores the outgoing digital television data and the incoming digital television data in an alternating manner,[13] and a memory controller that stores the incoming digital television data to one frame buffer and reads the outgoing digital television data from another frame buffer.[14] The graphics controller provides a feedback signal to the digital television/local bus interface logic to indicate whether a display device is refreshed.[15]

Yet still other embodiments are a digital television/local bus interface logic comprising a digital television interface that receives incoming digital television data,[16] a local bus interface that transmits outgoing digital television data to a graphics controller for display on a display device,[17] a first frame buffer that stores the incoming digital television data and the outgoing digital television data in an alternating manner,[18] a second frame buffer that stores the outgoing digital television data and the incoming digital television data in an alternating manner,[19] and a memory controller that stores the incoming digital television data to one frame buffer and reads the outgoing digital television data from another frame buffer on a first portion of a refresh of a display device and transmits the outgoing digital television data in the one frame buffer to the display device on a second

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[11] (7/13); Figure 3.

[12] (7/18-20); Figure 3.

[13] *Id.*

[14] (8/4-10); Figure 3.

[15] (5/33-6/2); Figure 2.

[16] (5/16-17); Figure 2.

[17] (5/17-18); Figure 2.

[18] (7/18-20); Figure 3.

[19] *Id.*

portion of the refresh of the display device,[20] the first and second portions of the refresh identified by a feedback signal from a graphics controller.[21]

Other illustrative embodiments are a digital television data handling system comprising[22] a first means for storing incoming digital television data and outgoing digital television data in an alternating manner,[23] a second means for storing the incoming digital television data and the outgoing digital television data in an alternating manner,[24] a means for monitoring a feedback signal[25] provided by a means for controlling graphics,[26] the feedback signal indicates whether a programmed position of a display device has been refreshed, and a means for transmitting the outgoing digital television data in one of the means for storing to the means for controlling graphics for display on the display device when a programmed position of the display device is refreshed.[27]

Other illustrative embodiments are a closed loop digital television data anti-tearing system comprising a central processing unit (CPU),[28] a local bus coupled to the CPU,[29] a graphics controller coupled to the local bus,[30] a display device that receives outgoing digital television data from the graphics controller,[31] and a digital television/local bus interface logic coupled to the local bus that stores incoming digital television data and the outgoing digital television data and selectively provides the outgoing digital television data over the local bus to the

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[20] (8/4-10); Figure 3.

[21] (5/33-6/2); Figure 6.

[22] Pursuant to 37 CFR 41.37, claim 34, to which this paragraph applies, is specifically identified to have means-plus-function limitations permitted under 35 USC § 112, sixth paragraph.

[23] (7/18-20); Figure 3.

[24] *Id.*

[25] (5/33-6/2); Figure 2.

[26] (5/21); Figure 2.

[27] (7/26-29; 8/4-10); Figures 2 and 3.

[28] (3/30); Figure 1.

[29] (5/18); Figure 2.

[30] (5/21); Figure 2.

[31] (5/27); Figure 2.

graphics controller when a programmed position of the display device is refreshed.[32] The graphics controller provides a feedback signal to the digital television/local bus interface logic to indicate whether a display device is refreshed.[33]

Finally, other illustrative embodiments are a closed loop digital television data anti-tearing system comprising a local bus,[34] a graphics controller coupled to the local bus,[35] a display device for receiving outgoing digital television data from the graphics controller,[36] and a digital television/local bus interface logic coupled to the local bus for storing incoming digital television data and the outgoing digital television data and selectively providing the outgoing digital television data over the local bus to the graphics controller when a programmed position of the display device is refreshed.[37] A refresh rate of the incoming digital television data is decoupled from a refresh rate of the outgoing digital television data, and wherein the graphics controller provides a feedback signal to the digital television/local bus interface logic to indicate whether the programmed position of the display device is refreshed.[38]

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[32] (7/33-8/22); Figures 2 and 3.

[33] (5/33-6/2); Figure 2.

[34] (5/18); Figure 2.

[35] (5/21); Figure 2.

[36] (5/27); Figure 2.

[37] (5/33-6/2); Figure 2.

[38] (5/33-6/11).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Whether claims 1-4, 6, 8-18, 20-24, 34-38 and 40-46 are unpatentable over Dye (U.S. Pat. No. 6,067,098).

VII. ARGUMENT

Before discussing specific rejections, Appellants present an overview of the Dye reference. The specific shortcomings of the reference with regard to the claimed subject matter will be discussed more fully below.

Dye is directed to a video/graphics controller which performs pointer-based display list video refresh operation.[39] Importantly for the determination to be made by the Board, Dye's concern is how to display data on a display screen once that data is in the system memory, not necessarily how that data gets to the system memory.

> First, **video data or pixel data is presumed to reside in the system memory 110** which is to be output onto the screen, ... This graphical or video data is written into the system memory 110 by the CPU 102 under the direction of a software program, such as an application program.[40]

In particular, Dye teaches that rather than moving large blocks of data from the system memory to a frame buffer for display, display refresh lists (which lists contain pointers to the pertinent data in the system memory) are used to gather the data for display.

> Thus it is noted that the present invention is not required to maintain, and preferably does not maintain, a single frame buffer which contains all of the video data for display on the video screen. Rather **the video data for the various windows and objects is stored in respective memory areas in the system memory 110, and pointers assembled in the display refresh list are used to reference this data during screen updates.** Thus, **data is not required to be moved in or out of a frame buffer to reflect screen changes, but rather in many instances either the video data for a respective window or object is changed, or only the pointers in the display refresh list are manipulated, to affect a screen change.**[41]

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[39] Dye Title.

[40] Dye Col. 23, lines 29-35 (emphasis added).

[41] Dye Col. 22, lines 53-65 (emphasis added).

To display video and/or pixel data once that data is in the system memory using the refresh lists, Dye discloses a hardware device that Dye titles an integrated memory controller (IMC).

> [T]he integrated memory control 140 of the present invention **integrates a memory controller and video and graphics controller capabilities into a single logical unit.**[42]

Thus, the IMC 140 of Dye is the video and graphics controller for the Dye system.

A. Claims 1-4

Claims 1-4 stands rejected as allegedly obvious over Dye. Claim 1 is representative of this grouping of claims. The grouping should not be construed to mean the patentability of any of the claims may be determined in later actions (*e.g.*, actions before a court) based on the groupings. Rather, the presumption of 35 USC § 282 shall apply to each of these claims individually.

Dye appears to teach an integrated device that acts as a memory controller and graphics controller.[43] Illustrative claim 1, by contrast, specifically recites, "storing incoming frames of digital television data in a first frame buffer **of an interface logic**; reading outgoing frames of digital television data from a second frame buffer **of the interface logic**; ... transmitting the outgoing frames of digital television data in the second frame buffer **to the graphics controller** to be displayed on the display device when the programmed position of the display device is refreshed." Appellants respectfully submit that Dye does not teach or fairly suggest the limitation of illustrative claim 1. Claim 1 clearly defines separate devices: an interface logic (having a first and second frame buffers); and a graphics controller (to which frames of digital television data are transmitted). Thus, Dye does not teach or fairly suggest the limitations of claim 1, and in fact Dye teaches away from the limitations by teaching integrated components. For this reason alone, the rejection of this grouping of claims should be overturned and the claims set for issue.

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[42] Dye Col. 10, lines 59-61 (emphasis added).

[43] Dye Col. 10, lines 59-61.

Further, Dye presumes the presence of pertinent data in the system memory, and is concerned with how to get video and/or pixel data from the system memory to the display device.[44] Appellants respectfully submit that because of the express presumption of Dye, Dye does not teach or fairly suggest, "transmitting the outgoing frames of digital television data in the second frame buffer [of an interface logic] to the graphics controller to be displayed on the display device when the programmed position of the display device is refreshed." It would appear that the teaching of Dye picks up only after the data arrives at the graphics controller. For this additional reason, alone or in combination with other shortcomings described in this section, the rejection of this grouping of claims should be overturned.

Further still, Dye teaches that, rather than transferring frames of video and/or pixel data for purposes of display, the video and/or pixel data should remain in the system memory and that display lists that contain pointers to pertinent system memory areas should be used.[45] Appellants therefore submit that either: Dye does not teach or fairly suggest "transmitting the outgoing **frames of digital television data**:..to the graphics controller... " as Dye appears to be concerned with aspects of displaying data once it arrives in the system memory; or that Dye that teaches away from, "transmitting the outgoing **frames of digital television data**... " inasmuch as Dye teaches using display lists rather than moving frames of data. For this additional reason, alone or in combination with other shortcomings described in this section, the rejection of this grouping of claims should be overturned.

Based on the forgoing, Appellants respectfully submit that the rejections of the claims in this first grouping be reversed, and the claims set for issue.

B. Claims 8-18, 20-24, 34-38 and 40-46

Claims 8-18, 20-24, 34-38 and 40-46 stand rejected as allegedly obvious over Dye. Claim 8 is illustrative of this grouping of claims. The grouping should

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[44] Dye Col. 23, lines 29-35.

[45] Dye Col. 22, lines 53-65 (emphasis added).

not be construed to mean the patentability of any of the claims may be determined in later actions (*e.g.*, actions before a court) based on the groupings. Rather, the presumption of 35 USC § 282 shall apply to each of these claims individually.

Dye appears to teach an integrated device that acts as a memory controller and graphics controller.[46] Illustrative claim 8, by contrast specifically recites, "a graphics controller coupled to the CPU; [and] digital television/local bus interface logic coupled to the graphics controller by way of the local bus... ." Appellants respectfully submit that Dye does not teach or fairly suggest the limitation of illustrative claim 8. Claim 8 defines separate devices: a graphics controller; and a digital television/local bus interface logic coupled to the graphics controller by way of the local bus. If Dye's integrated memory controller 140 (which Dye teaches is both a memory controller and a graphic controller) is the claimed graphics controller, then Dye fails to teach the "digital television/local bus interface logic coupled to the graphics controller by way of the local bus." On the other hand, if Dye's integrated memory controller 140 is the claimed digital television/local bus interface, then Dye fails to teach the separately claimed graphics controller. For this reason alone, the rejection of this grouping of claims should be overturned and the claims set for issue.

Further, Dye presumes the presence of pertinent data in the system memory, and is concerned with how to get video and/or pixel data from a system memory to the display device.[47] Appellants respectfully submit that because of the express presumption of Dye, Dye does not teach or fairly suggest "a graphics controller coupled to the CPU; digital television/local bus interface logic coupled to the graphics controller **by way of the local bus**... [the] digital television/local bus interface logic comprising: ... a local bus interface **that transmits outgoing digital television data to the graphics controller over the local bus**... ." It appears that the teaching of Dye picks up only after the data arrives at the

[46] Dye Col. 10, lines 59-61.

[47] Dye Col. 23, lines 29-35.

graphics controller. For this additional reason, alone or in combination with other shortcomings described in this section, the rejection of this grouping of claims should be overturned.

Further still, Dye teaches that, rather than transferring frames of video and/or pixel data for purposes of display, the video and/or pixel data should remain in the system memory and that display lists that contain pointers to pertinent system memory areas should be used.[48] Appellants therefore submit that Dye teaches away from, "a graphics controller ...; digital television/local bus interface logic coupled to the graphics controller by way of the local bus... [the] digital television/local bus interface logic comprising: ... **a first frame buffer** that stores the incoming digital television data and the outgoing digital television data in an alternating manner; **a second frame buffer** that stores the outgoing digital television data and the incoming digital television data in an alternating manner; and a memory controller that stores the incoming digital television data to one frame buffer and **reads the outgoing digital television data from another frame buffer**." Dye teaches against frame-based operations. For this additional reason, alone or in combination with other shortcomings described in this section, the rejection of this grouping of claims should be overturned.

Further still, because of the presumption of presence of the video and/or pixel data, and the corresponding lack of teaching of how video and/or pixel data arrives in the system memory, Dye is apparently unconcerned with timing of the arrival of video and/or pixel data in the system memory in relation to refresh of the display.[49] Illustrative claim 8, by contrast, specifically recites, "wherein the graphics controller provides a feedback signal to the digital television/local bus interface logic to indicate whether a display device is refreshed." Dye mentions signals such as horizontal and vertical synchronization signals,[50] but fails to show them in the Dye figures, and further fails to teach or fairly suggest that signals

[48] Dye Col. 22, lines 53-65 (emphasis added).

[49] Dye Col. 23, lines 29-35; *see* Col. 23, lines 32-35.

[50] Dye Col. 18, lines 51-52.

such as these should be provided by the Dye graphics controller to a device coupled to the graphics controller across a local bus. For this additional reason, alone or in combination with other shortcomings described in this section, the rejection of this grouping of claims should be overturned and the claims set for issue.

Based on the forgoing, Appellants respectfully submit that the rejections of the claims in this second grouping be reversed, and the grouping set for issue.

VIII. CONCLUSION

For the reasons stated above, Appellants respectfully submit that the Examiner erred in rejecting all pending claims. It is believed that no extensions of time or fees are required, beyond those that may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary to allow consideration of this paper, such extensions are hereby petitioned under 37 CFR § 1.136(a), and any fees required (including fees for net addition of claims) are hereby authorized to be charged to Hewlett-Packard Development Company's Deposit Account No. 08-2025.

Respectfully submitted,

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IX. CLAIMS APPENDIX

1. (Previously presented) A method comprising:

storing incoming frames of digital television data in a first frame buffer of an interface logic;

reading outgoing frames of digital television data from a second frame buffer of the interface logic;

monitoring a feedback signal provided by a graphics controller coupled to the system, the monitoring by the interface logic and the feedback signal indicates whether a programmed position of a display device has been refreshed; and

transmitting the outgoing frames of digital television data in the second frame buffer to the graphics controller to be displayed on the display device when the programmed position of the display device is refreshed.

2. (Previously presented) The method of claim 1, further comprising:

storing the incoming frames of digital television data in the second frame buffer;

reading the outgoing frames of digital television data from the first frame buffer; and

transmitting the outgoing frames of digital television data in the first frame buffer to the display device when the programmed position of the display device is refreshed.

3. (Previously presented) The method of claim 1, further comprising:

detecting whether the outgoing frames of digital television data is stored in the first frame buffer or the second frame buffer.

4. (Previously presented) The method of claim 1, the monitoring further comprising:

monitoring a horizontal sync and a vertical sync of the display device.

5. (Cancelled).

6. (Previously presented) The method of claim 1, the transmitting further comprising:

transmitting the outgoing frames of digital television data over a peripheral component interconnect (PCI) bus.

7. (Cancelled).

8. (Previously presented) A system comprising:

a central processing unit (CPU);

a graphics controller coupled to the CPU;

a local bus coupled to the CPU and graphics controller; and

digital television/local bus interface logic coupled to the graphics controller by way of the local bus, the digital television/local bus interface logic comprising:

a digital television interface that receives incoming digital television data;

a local bus interface that transmits outgoing digital television data to the graphics controller over the local bus;

a first frame buffer that stores the incoming digital television data and the outgoing digital television data in an alternating manner;

a second frame buffer that stores the outgoing digital television data and the incoming digital television data in an alternating manner; and

a memory controller that stores the incoming digital television data to one frame buffer and reads the outgoing digital television data from another frame buffer

wherein the graphics controller provides a feedback signal to the digital television/local bus interface logic to indicate whether a display device is refreshed.

9. (Original) The system of claim 8, wherein the local bus comprises a peripheral component interconnect (PCI) bus.

10. (Original) The system of claim 8, further comprising:
a display device coupled to the local bus for receiving outgoing digital television data over the local bus.

11. (Previously presented) The system of claim 8, wherein the memory controller stores the incoming digital television data to the first frame buffer and reads the outgoing digital television data from the second frame buffer on a first portion of a refresh of the display device and transmits the outgoing digital television data in the second frame buffer to the display device on a second portion of the refresh of the display device.

12. (Previously presented) The system of claim 8, wherein the memory controller stores the incoming digital television data to the second frame buffer and reads the outgoing digital television data from the first frame buffer on a first portion of a refresh of the display device and transmits the outgoing digital television data in the first frame buffer to the display device on a second portion of the refresh of the display device.

13. (Previously presented) The system of claim 8, wherein the local bus interface monitors a refresh of the display device for receiving the outgoing digital television data.

14. (Original) The system of claim 8, wherein a refresh rate of the incoming digital television data is decoupled from a refresh rate of the outgoing digital television data.

15. (Original) The system of claim 8, the digital television/local bus logic further comprising:

a write state machine for detecting whether the incoming digital television data is being written to the first frame buffer or the second frame buffer.

16. (Original) The system of claim 8, the digital television/local bus logic further comprising:

a read state machine for informing the memory controller of a frame buffer from which to read the outgoing digital television data.

17. (Previously presented) A digital television/local bus interface logic, comprising:

a digital television interface that receives incoming digital television data;

a local bus interface that transmits outgoing digital television data to a graphics controller for display on a display device;

a first frame buffer that stores the incoming digital television data and the outgoing digital television data in an alternating manner;

a second frame buffer that stores the outgoing digital television data and the incoming digital television data in an alternating manner; and

a memory controller that stores the incoming digital television data to one frame buffer and reads the outgoing digital television data from another frame buffer on a first portion of a refresh of a display device and transmits the outgoing digital television data in the one frame buffer to the display device on a second portion of the refresh of the display device, the first and second portions of the refresh identified by a feedback signal from a graphics controller.

18. (Original) The interface logic of claim 17, wherein the local bus interface comprises a peripheral component interconnect (PCI) interface.

19. (Cancelled).

20. (Original) The interface logic of claim 17, wherein the memory controller stores the incoming digital television data to the first frame buffer and reads the outgoing digital television data from the second frame buffer on a first portion of a refresh of the display device and transmits the outgoing digital television data in the second frame buffer to the display device on a second portion of the refresh of the display device.

21. (Original) The interface logic of claim 17, wherein the memory controller stores the incoming digital television data to the second frame buffer and reads the outgoing digital television data from the first frame buffer on a first portion of a refresh of the display device and transmits the outgoing digital television data in the first frame buffer to the display device on a second portion of the refresh of the display device.

22. (Original) The interface logic of claim 17, wherein a refresh rate of the incoming digital television data is decoupled from a refresh rate of the outgoing digital television data.

23. (Original) The interface logic of claim 17, further comprising:
a write state machine for detecting whether the incoming digital television data is being written to the first frame buffer or the second frame buffer.

24. (Original) The interface logic of claim 17, further comprising:
a read state machine for informing the memory controller of a frame buffer from which to read the outgoing digital television data.

25.-33. (Cancelled).

34. (Previously presented) A digital television data handling system, comprising:

a first means for storing incoming digital television data and outgoing digital television data in an alternating manner;

a second means for storing the incoming digital television data and the outgoing digital television data in an alternating manner;

a means for monitoring a feedback signal provided by a means for controlling graphics, the feedback signal indicates whether a programmed position of a display device has been refreshed; and

a means for transmitting the outgoing digital television data in one of the means for storing to the means for controlling graphics for display on the display device when a programmed position of the display device is refreshed.

35. (Previously presented) The system of claim 34, the means for transmitting comprising:

a means for reading the outgoing digital television data from one of the means for storing.

36. (Previously presented) The system of claim 34, the means for monitoring comprising:

a means for monitoring a horizontal sync and a vertical sync of the display device.

37. (Previously presented) The system of claim 34, the means for transmitting comprising:

a means for detecting whether the outgoing digital television data is stored in the first means for storing or the second means for storing.

38. (Previously presented) The system of claim 34, the means for transmitting comprising:

a means for transmitting the outgoing digital television data over a peripheral component interconnect (PCI) bus.

39. (Cancelled).

40. (Previously presented) A closed loop digital television data anti-tearing system, comprising:

a central processing unit (CPU);

a local bus coupled to the CPU;

a graphics controller coupled to the local bus;

a display device that receives outgoing digital television data from the graphics controller; and

a digital television/local bus interface logic coupled to the local bus that stores incoming digital television data and the outgoing digital television data and selectively provides the outgoing digital television data over the local bus to the graphics controller when a programmed position of the display device is refreshed;

wherein the graphics controller provides a feedback signal to the digital television/local bus interface logic to indicate whether a display device is refreshed.

41. (Original) The anti-tearing system of claim 40, further comprising:

a core logic coupled between the local bus and the graphics controller.

42. (Original) The anti-tearing system of claim 40, further comprising:

a digital television decoder for providing incoming television data to the digital television/local bus interface logic.

43. (Original) The anti-tearing system of claim 42, further comprising:

a digital television tuner for providing incoming digital television data to the digital television decoder.

44. (Previously presented) A closed loop digital television data anti-tearing system, comprising:

a local bus;

a graphics controller coupled to the local bus;

a display device for receiving outgoing digital television data from the graphics controller; and

a digital television/local bus interface logic coupled to the local bus for storing incoming digital television data and the outgoing digital television data and selectively providing the outgoing digital television data over the local bus to the graphics controller when a programmed position of the display device is refreshed,

wherein a refresh rate of the incoming digital television data is decoupled from a refresh rate of the outgoing digital television data, and wherein the graphics controller provides a feedback signal to the digital television/local bus interface logic to indicate whether the programmed position of the display device is refreshed.

45. (Original) The anti-tearing system of claim 44, wherein the feedback signal comprises a horizontal sync and a vertical sync of the display device.

46. (Original) The anti-tearing system of claim 40, wherein the local bus comprises a peripheral component interconnect (PCI) bus.

47. (Cancelled).

48. (Original) A dual stream digital television/local bus interface logic, comprising:

a first digital television interface for receiving a first incoming digital television data stream;

a second digital television interface for receiving a second incoming digital television data stream;

a local bus interface for transmitting a first outgoing digital data stream and a second outgoing digital television data stream;

a first frame buffer for storing the first incoming digital television data stream and the first outgoing digital television data stream in an alternating manner;

a second frame buffer for storing the first outgoing digital television data stream and the first incoming digital television data stream in an alternating manner;

a third frame buffer for storing the second incoming digital television data stream and the second outgoing digital television data stream in an alternating manner;

a fourth frame buffer for storing the second outgoing digital television data stream and the second incoming digital television data stream in an alternating manner; and

a memory controller for storing the first incoming digital television data stream to the first frame buffer or the second frame buffer and reading the first outgoing digital television data stream from the second frame buffer or the first frame buffer on a first portion of a refresh of a display device, storing the second incoming digital television data stream to the third frame buffer or the fourth frame buffer and reading the second outgoing digital television data stream from the fourth frame buffer or the third frame buffer on the first portion of the refresh of the display device, transmitting the first outgoing digital television data stream to the display device on a second portion of the refresh of the display device, and

transmitting the second outgoing digital television data stream to the display device on the second portion of the refresh of the display device.

49. (Original) The interface logic of claim 48, wherein the local bus interface comprises a peripheral component interconnect (PCI) interface.

50. (Original) The interface logic of claim 48, wherein a refresh rate of the first outgoing digital television data stream is decoupled from a refresh rate of the first incoming digital television stream and a refresh rate of the second outgoing digital television data stream is decoupled from the refresh rate of the second incoming digital television data stream.

51. (Original) The interface logic of claim 48, further comprising:

a local bus interface buffer for receiving and storing the first outgoing digital television data stream from the first frame buffer and the second frame buffer and for receiving and storing the second outgoing digital television data stream from the third frame buffer and the fourth frame buffer.

52. (Original) The interface logic of claim 48, further comprising:

a first set of digital television interface buffers coupled to the first digital television interface for receiving a first incoming digital television data stream; and

a second set of digital television interface buffers coupled to the second digital television interface for receiving the second incoming digital television data stream.

53.-61. (Cancelled).

X. EVIDENCE APPENDIX

None.

XI. RELATED PROCEEDINGS APPENDIX

None.